Attorney Docket No. 5649-1159 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Gi-ho Park
Application No.: 10/801,893
Filed: March 16, 2004
For: *Methods, Circuits, and Systems for Utilizing Idle Time in Dynamic Frequency Scaling Cache Memories*

Confirmation No.: 3389
Group Art Unit: 2187
Examiner: Than Vinh Nguyen

Date: April 26, 2007

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Sir:

Attached is a list of documents, together with a copy of any listed foreign patent document and/or non-patent literature. A copy of any listed U.S. patent and/or U.S. patent application publication is not provided herewith in accordance with the amendment by the U.S. Patent and Trademark Office to 37 C.F.R. § 1.98(a)(2)(ii) effective October 21, 2004. It is requested that these documents be considered by the Examiner and officially made of record in accordance with the provisions of 37 C.F.R. § 1.56 and Section 609 of the MPEP.

This Information Disclosure is submitted in accordance with 37 C.F.R. § 1.97(b)(4), before the mailing of a first action after the filing of a Request for Continued Examination under 37 C.F.R. § 1.114. Therefore, no fee is believed due. However, the Commissioner is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 50-0220.

Respectfully submitted,

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CERTIFICATION OF TRANSMISSION

I hereby certify that this correspondence is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4) to the U.S. Patent and Trademark Office on April 26, 2007.

Sheena Donnelly

INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Complete if Known	
				Application Number	10/801,893
				Filing Date	March 16, 2004
				First Named Inventor	Gi-ho Park
				Group Art Unit	2187
(use as many sheets as necessary)				Examiner Name	Than Vinh Nguyen
Sheet	1	of	A1	Attorney Docket Number	5649-1159

U.S. PATENTS AND PATENT PUBLICATIONS					
Examiner Initials*	Cite No.	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY
		Number	Kind Code (if known)		
		US-			
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FOREIGN PATENT DOCUMENTS							
Examiner Initials*	Cite No.	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Translation
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OTHER NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T
	1.	Ghose et al. "Reducing Power in Superscalar Processor Caches Using Subbanking, Multiple Line Buffers and Bit-Line Segmentation" *Proceedings Of The 1999 International Symposium On Low Power Electronics And Design* pp. 70-75 (1999)	
	2.	Hennessy et al. *Computer Architecture: A Quantitative Approach*, 3rd Edition, chapter 3.11 "Another View: Thread-Level Parallelism" Morgan Kaufmann Publishers, San Francisco, CA (2003)	
	3.	Kin et al. "The Filter Cache: An Energy Efficient Memory Structure" *Proceedings of the Thirtieth Annual IEEE/ACM International Symposium on Microarchitecture,* pp. 184-193, (1997)	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.